CLAIM LISTING:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween;

a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region;

a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers;

a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and

a third impurity doped layer of the first conductivity type formed under said second impurity doped layer, wherein

said three impurity doped layers make up a multilayer lamination structure with two ~~junctions therebetween~~ p-n junctions, one between said first and said second impurity doped layers and the other between said second and said third impurity doped layer, wherein

said first impurity doped layer is equal to or less in junction depth than the extension region of each of said source/drain diffusion layers, and wherein

said second impurity doped layer is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first and third impurity doped layers.

2. (Original) The device according to claim 1, wherein said first impurity doped layer is set in impurity concentration and thickness to be fully depleted upon formation of a channel inversion layer.

3. (Original) The device according to claim 1, wherein said first impurity doped layer is set in impurity concentration and thickness to be partially depleted upon formation of a channel inversion layer.

4. (Original) The device according to claim 1, wherein each of said first and second impurity doped layers is formed by ion implantation of an impurity into an undoped semiconductor layer as has been epitaxially grown on said semiconductor substrate with said third impurity doped layer formed therein.

5. (Original) The device according to claim 1, wherein said second impurity doped layer is selectively formed in a region immediately beneath said gate electrode.

6. (Original) The device according to claim 4, wherein

said second impurity doped layer is selectively formed in a region of said undoped semiconductor layer just beneath said gate electrode, and wherein

said source/drain diffusion layers are formed so that a bottom surface of the low resistivity region resides within said undoped semiconductor layer whereas a bottom surface of the extension region is in contact with said second impurity doped layer.

7. (Original) The device according to claim 1, further comprising:

fourth impurity doped layers of the first conductivity type as embedded to be in contact with the extension regions of said source and drain diffusion layers.

8. (Original) The device according to claim 1, wherein the low resistivity regions of said source/drain diffusion layers are formed to have top surfaces higher in level than said gate dielectric film.

9. (Original) The device according to claim 1, wherein said gate electrode has a metal film as contacted with the gate dielectric film.

10. (Original) The device according to claim 2, wherein said gate electrode is formed of a metal film.

11. (Original) The device according to claim 3, wherein said gate electrode is formed of a poly-silicon film.

12-42. (Cancelled)

REMARKS

Claims 1-11 are pending. Claim 1 has been amended. Claims 12-42 have been cancelled without prejudice or disclaimer as to Applicants right to pursue the subject matter of these claims in a continuing application. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Entry of this amendment is respectfully requested as no new search is required and it places the application in a condition for allowance or at least in better form for appeal.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 4, 5, and 11 were rejected under 35 U.S.C. § 102(a) over Kawashima (U.S. Patent No. 6,163,053). Applicant respectfully traverses this rejection.

Claim 1 recites, in part, a semiconductor device which includes three impurity doped layers that make up a multilayer lamination structure with two p-n junctions, one between the first and the second impurity doped layers and the other between the second and third impurity doped layer. In contrast, Kawashima discloses a channel region 19, an opposite polarity region 156, and a well region 15 which the Office Action alleges corresponds to the first second and third impurity doped layer of claim 1, respectively. Even if this were the case, the channel region 19 and the opposite polarity region 156 do not share a p-n junction since they are separated by the well region 15 (Figure 6c). Accordingly, Kawashima does not teach that the three layers make up a multilayer lamination structure with two p-n junctions, one between the first and the second impurity doped layers and the other between the second and third impurity doped layer, as recited in claim 1.

Claims 4, 5, and 11 are believed allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claim Rejections Under 35 U.S.C. § 103

A. Claims 2 and 3 were rejected under 35 U.S.C. § 103(a) over Kawashima. Applicant respectfully traverses this rejection.

Claims 2 and 3 are believed allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

B. Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) over Kawashima in view of Cheek et al. (U.S. Patent No. 6,162,694). Applicant respectfully traverses this rejection.

Claims 9 and 10 are believed allowable for at least the reasons presented above with regard to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Conclusion

In view of the foregoing, the claims are believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Please charge any fees associated with the submission of this paper to Deposit Account Number 03-3975 under Order No. 44020/284163. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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